REMARKS

This is in full and timely response to the Office Action dated January 28, 2009.

Claims 17-26 are currently pending in this application, with claim 17 being independent.

No new matter has been added.

Reexamination in light of the following remarks is respectfully requested.

Prematureness

Applicant, seeking review of the *prematureness* of the final rejection within the Final Office Action, respectfully requests reconsideration of the finality of the Final Office Action for the reasons set forth hereinbelow. See M.P.E.P. §706.07(c).

At least for the following reasons, if the allowance of the claims is not forthcoming at the very least and a new ground of rejection made, then a ***new non-final Office Action*** is respectfully requested.

Rejections under 35 U.S.C. §102 and 35 U.S.C. §103

Paragraph 2 indicates a rejection of claims 17, 18 and 23-25 under 35 U.S.C. §102 as allegedly being anticipated by U.S. Patent No. 6,56,7066 (Hashimoto).

Paragraph 4 indicates a rejection of claims 19-22 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 6,56,7066 (Hashimoto) in view of U.S. Patent No. 6,313,819 (Maekawa).

Paragraph 5 indicates a rejection of claim 26 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 6,56,7066 (Hashimoto) in view of U.S. Patent No. 6,091,391 (Ling).

These rejections are traversed at least for the following reasons.

Claims 17-26 - Claims 18-26 are dependent upon claim 17. Claim 17 is drawn to a display device comprising:

> a matrix of pixels, a pixel of said matrix of pixels having an electro-optic material between a pixel electrode and a common electrode;
>
> a common driver having an offset circuit, a common voltage generated by said common driver being applied to said common electrode,
>
> wherein said offset circuit is charged to an offset voltage at a time of a rising edge of a power supply voltage, said offset voltage adjusting a level of said common voltage.

Hashimoto - Hashimoto arguably discloses gray shade voltages VX0-VX9 (Hashimoto at Figures 1, 2, 9, 10).

However, Hashimoto ***fails*** to disclose, teach, or suggest that the output offset control circuit 14 is charged to an offset voltage at a time of a rising edge of any of the gray shade voltages VX0-VX9.

Hashimoto arguably discloses supply voltage VDD (Hashimoto at Figure 5).

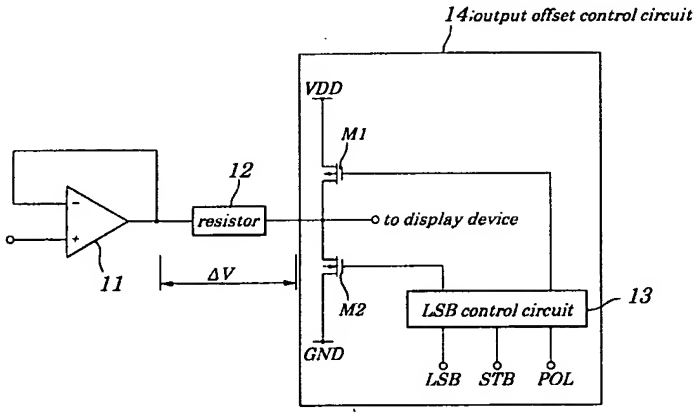
However, Hashimoto ***fails*** to disclose, teach, or suggest that the output offset control circuit 14 is charged to an offset voltage at a time of a rising edge of supply voltage VDD.

Instead, the Office Action contends that Hashimoto discloses a device wherein said offset circuit is charged to an offset voltage at a time of a rising edge of a power supply voltage

(Fig. 5, M1 which is connected to VDD and Fig. 6, offset circuit is charged when M1 is on), said offset voltage adjusting a level of said common voltage (Fig. 6(ΔV)) (Office Action at page 2).

In response, Figure 5 of Hashimoto is provided hereinbelow.

FIG.5

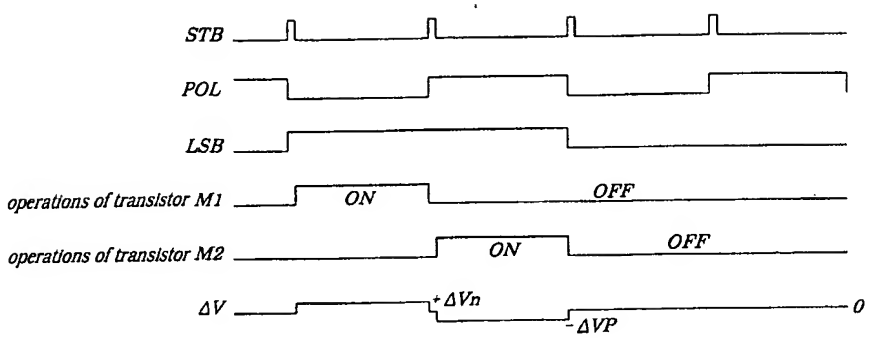


Hashimoto arguably discloses at column 7, lines 7-23, that:

> FIG. 5 is a schematic block diagram showing first and second output circuits shown in FIG. 1. Each of the output circuits is provided with an operational amplifier 11 used to amplify an output signal fed from the gray shade voltage selecting circuit and to convert its impedance. Between the operational amplifier 11 and an output terminal connected to the display device is connected a resistor 12 including an analog switch or the like. Between the resistor 12 and the output terminal are connected transistors M1 and M2 drains of which are connected to each other. A source of the transistor M1 is connected to a terminal of supply voltage VDD and a source of the transistor M2 is connected to a ground GND. Gates of the transistors M1 and M2 are connected to an LSB control circuit 13. To the LSB control circuit 13 are inputted the least significant bit (1 bit) of the digital image data and polarity signal POL and latch signal STB. That is, *an output offset control circuit 14 is composed of transistors M1 and M2 and of the LSB control circuit 13*.

Figure 6 of Hashimoto is provided hereinbelow.

FIG.6



Hashimoto arguably discloses at column 8, lines 13-21, that:

> FIG. 6 is a time chart showing operations of the first output circuit 9 according to the first embodiment. In the first output circuit 9, if the least significant bit LSB is 0 (low), both of the transistors M1 and M2 are turned OFF regardless of the polarity signal POL. At this point, the voltage drop in the resistor 12 including analog switches or the like does not occur because currents do not flow constantly, an output voltage supplied from the operational amplifier 11, as it is, is applied to the display device from the output terminal.

Here, the transistors M1 and M2 of Hashimoto are switched ON or OFF by the LSB control circuit 13 ***based on the least significant bit of the digital image data*** (Hashimoto at column 7, lines 29-31).

In this regard, the Office Action ***fails*** to show that *the least significant bit of the digital image data* of Hashimoto and a *power supply voltage* are one in the same, especially when Figure 5

of Hashimoto appears to depict the least significant bit LSB as being something other than supply voltage VDD.

Likewise, Figure 6 of Hashimoto ***fails*** to show the switching of either transistor M1 or transistor M2 on a rising edge of any signal.

- ***Thus, Hashimoto fails to disclose, teach, or suggest a device wherein said offset circuit is charged to an offset voltage at a time of a rising edge of a power supply voltage, said offset voltage adjusting a level of said common voltage.***

Maekawa - The Office Action cites Maekawa for the features that are deficient from within Hashimoto.

However, the Office Action ***fails*** to show within Maekawa the presence of a rising edge of a power supply voltage VCC.

- ***Thus, the Office Action fails to show that Maekawa discloses a device wherein said offset circuit is charged to an offset voltage at a time of a rising edge of a power supply voltage, said offset voltage adjusting a level of said common voltage.***

Ling - The Office Action cites Ling for the features that are deficient from within Hashimoto.

However, no timing diagram can be found within Ling.

- ***Thus, Ling fails to disclose, teach, or suggest a device wherein said offset circuit is charged to an offset voltage at a time of a rising edge of a power supply voltage, said offset voltage adjusting a level of said common voltage.***

Withdrawal of these rejections and allowance of the claims is respectfully requested.

Official Notice

There is no concession as to the veracity of Official Notice, if taken in any Office Action.

An affidavit or document should be provided in support of any Official Notice taken. 37 CFR 1.104(d)(2), MPEP § 2144.03. See also, *Ex parte Natale*, 11 USPQ2d 1222, 1227-1228 (Bd. Pat. App. & Int. 1989)(failure to provide any objective evidence to support the challenged use of Official Notice constitutes clear and reversible error).

Extensions of time

Please treat any concurrent or future reply, requiring a petition for an extension of time under 37 C.F.R. §1.136, as incorporating a petition for extension of time for the appropriate length of time.

Fees

The Commissioner is hereby authorized to charge any deficiency in fees filed, asserted to be filed, or which should have been filed herewith (or with any paper hereafter filed in this application by this firm).

The Commissioner is hereby authorized to charge all required fees, fees under 37 C.F.R. §1.17, or all required extension of time fees.

If any fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

Conclusion

This response is believed to be a complete response to the Office Action.

Applicants reserve the right to set forth further arguments supporting the patentability of their claims, including the separate patentability of the dependent claims not explicitly addressed herein, in future papers.

For the foregoing reasons, all the claims now pending in the present application are allowable, and the present application is in condition for allowance.

Accordingly, favorable reexamination and reconsideration of the application in light of the remarks is courteously solicited.

If the Examiner has any comments or suggestions that could place this application in even better form, the Examiner is requested to telephone Brian K. Dutton, Reg. No. 47,255, at 202-955-8753.

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Respectfully submitted,

By 40,290

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